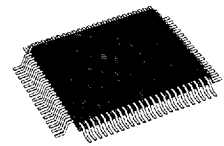
SGS-THOMSON MICROELECTRONICS

ST90E40
ST90T40

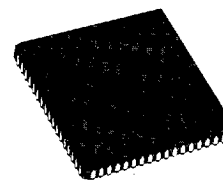
16K EPROM HCMOS MCU WITH EEPROM, RAM AND A/D CONVERTER

PRELIMINARY DATA

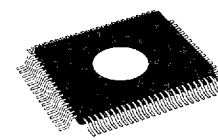
- Register oriented 8/16 bit CORE with RUN, WFI and HALT modes
- Minimum instruction cycle time: 500ns (12MHz internal)
- Internal Memory :
  EPROM 16K bytes
  RAM 256 bytes
  EEPROM 512 bytes
  224 general purpose registers available as RAM, accumulators or index pointers (Register File)
- 80-pin Plastic Quad Flat Pack package for ST90T40Q
- 68-lead Plastic Leaded Chip Carrier package for ST90T40C
- 80-pin Windowed Ceramic Quad Flat Pack package for ST90E40G
- 68-lead Windowed Ceramic Leaded Chip Carrier package for ST90E40L
- DMA controller, Interrupt handler and Serial Peripheral Interface as standard features
- 56 fully programmable I/O pins
- Up to 8 external plus 1 non-maskable interrupts
- 16 bit Timer with 8 bit Prescaler, able to be used as a Watchdog Timer
- Two 16 bit Multifunction Timers, each with an 8 bit prescaler and 13 operating modes
- 8 channel 8 bit Analog to Digital Converter, with Analog Watchdogs and external references
- Serial Communications Interface with asynchronous and synchronous capability
- Rich Instruction Set and 14 Addressing modes
- Division-by-Zero trap generation
- Versatile Development tools, including assembler, linker, C-compiler, archiver, graphic oriented debugger and hardware emulators
- Real Time Operating System
- Compatible with ST9040 16K ROM device



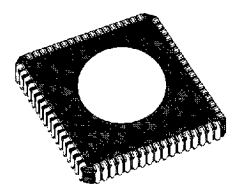
PQFP80



PLCC68



CQFP80W



CLCC68W

(Ordering Information at the end of the Datasheet)

Figure 1. 80 Pin QFP Package

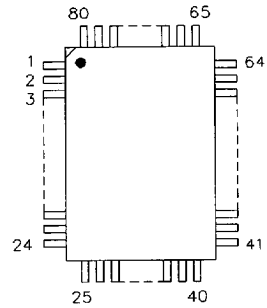


Table 1. ST90E40G-ST90T40Q Pin Description

Pin	Name
1	AV_{SS}
2	AV_{SS}
3	NC
4	P44/Ain4
5	P57
6	P56
7	P55
8	P54
9	INT7
10	INT0
11	P53
12	NC
13	P52
14	P51
15	P50
16	OSCOUT
17	V_{SS}
18	V_{SS}
19	NC
20	OSCIN
21	$\overline{RESET}/V_{PP}$
22	P37/T1OUTB
23	P36/T1INB
24	P35/T1OUTA

Pin	Name
25	P34/T1INA
26	P33/T0OUTB
27	P32/T0INB
28	P31/T0OUTA
29	P30/P/$\overline{D}$/T0INA
30	P17/A15
31	P16/A14
32	NC
33	P15/A13
34	P14/A12
35	P13/A11
36	P12/A10
37	P11/A9
38	P10/A8
39	P00/A0/D0
40	P01/A1/D1

Pin	Name
64	P20/NMI
63	NC
62	V_{SS}
61	P70/SIN
60	P71/SOUT
59	P72/INT4/TXCLK /CLKOUT
58	P73/INT5 /RXCLK/ADTRG
57	P74/P/$\overline{D}$/INT6
56	P75/$\overline{WAIT}$
55	P76/WDOUT /BUSREQ
54	P77/WDIN /BUSACK
53	R/$\overline{W}$
52	NC
51	$\overline{DS}$
50	$\overline{AS}$
49	NC
48	V_{DD}
47	V_{DD}
46	P07/A7/D7
45	P06/A6/D6
44	P05/A5/D5
43	P04/A4/D4
42	P03/A3/D3
41	P02/A2/D2

Pin	Name
80	AV_{DD}
79	NC
78	P47/Ain7
77	P46/Ain6
76	P45/Ain5
75	P43/Ain3
74	P42/Ain2
73	P41/Ain1
72	P40/Ain0
71	P27/RRDY5
70	P26/$\overline{INT3}$ /$\overline{RDSTB5}$/P/$\overline{D}$
69	P25/WRRDY5
68	P24/$\overline{INT1}$ /$\overline{WRSTB5}$
67	P23/SDO
66	P22/INT2/SCK
65	P21/SDI/P/$\overline{D}$

Figure 2. 68 Pin LCC Package

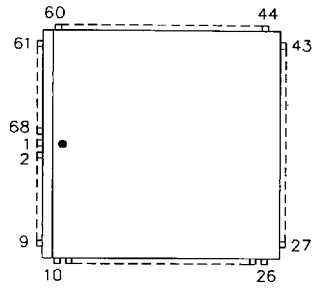


Table 2. ST90E40L-ST90T40C

Pin	Name
61	P44/Ain4
62	P57
63	P56
64	P55
65	P54
66	INT7
67	INT0
68	P53
1	P52
2	P51
3	P50
4	OSCOUT
5	V_{SS}
6	OSCIN
7	$\overline{RESET}/V_{PP}$
8	P37/T1OUTB
9	P36/T1INB

Pin	Name
10	P35/T1OUTA
11	P34/T1INA
12	P33/T0OUTB
13	P32/T0INB
14	P31/T0OUTA
15	P30/P/$\overline{D}$/T0INA
16	P17/A15
17	P16/A14
18	P15/A13
19	P14/A12
20	P13/A11
21	P12/A10
22	P11/A9
23	P10/A8
24	P00/A0/D0
25	P01/A1/D1
26	P02/A2/D2

Pin	Name
43	P70/SIN
42	P71/SOUT
41	P72/CLKOUT /TXCLK/INT4
40	P73/ADTRG /RXCLK/INT5
39	P74/P/$\overline{D}$/INT6
38	$\overline{P75}/\overline{WAIT}$
37	P76/WDOUT /$\overline{BUSREQ}$
36	P77/WDIN /$\overline{BUSACK}$
35	R/$\overline{W}$
34	DS
33	$\overline{AS}$
32	V_{DD}
31	P07/A7/D7
30	P06/A6/D6
29	P05/A5/D5
28	P04/A4/D4
27	P03/A3/D3

Pin	Name
60	AV_{SS}
59	AV_{DD}
58	P47/Ain7
57	P46/Ain6
56	P45/Ain5
55	P43/Ain3
54	P42/Ain2
53	P41/Ain1
52	P40/Ain0
51	P27/RRDY5
50	P26/INT3 /RDSTB5/P/D
49	P25/WRRDY5
48	P24/INT1 /WRSTB5
47	P23/SDO
46	P22/INT2/SCK
45	P21/SDI/P/$\overline{D}$
44	P20/NMI

1.1 GENERAL DESCRIPTION

The ST90E40 and ST90T40 (following mentioned as ST90E40)are EPROM members with EEPROM of the ST9 family of microcontrollers, in windowed ceramic (E) and plastic OTP (T) packages respectively, completely developed and produced by SGS-THOMSON Microelectronics using a n-well proprietary HCMOS process.

The EPROM parts are fully compatible with their ROM versions and this datasheet will thus provide only information specific to the EPROM based devices.

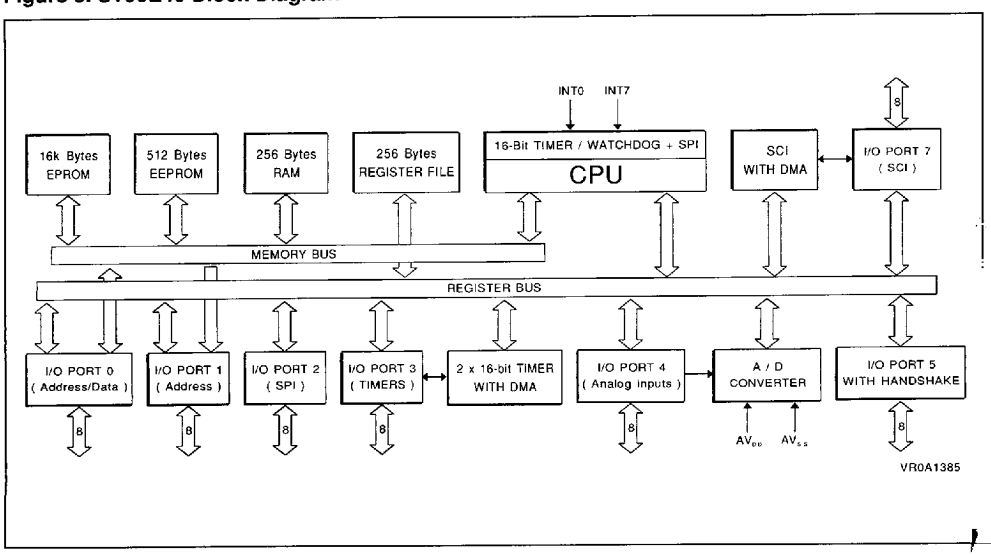
THE READER IS ASKED TO REFER TO THE DATASHEET OF THE ST9040 ROM-BASED DEVICE FOR FURTHER DETAILS.

The EPROM ST90E40 may be used for the prototyping and pre-production phases of development, and can be configured as: a standalone microcontroller with 16K bytes of on-chip ROM, a microcontroller able to manage external memory, or as a parallel processing element in a system with other processors and peripheral controllers.

The nucleus of the ST90E40 is the advanced Core which includes the Central Processing Unit (CPU), the Register File, a 16 bit Timer/Watchdog with 8 bit Prescaler, a Serial Peripheral Interface supporting S-bus, I^2C-bus and IM-bus Interface, plus two 8 bit I/O ports. The Core has independent memory and register buses allowing a high degree of pipelining to add to the efficiency of the code execution speed of the extensive instruction set.

The powerful I/O capabilities demanded by microcontroller applications are fulfilled by the ST90E40 with up to 56 I/O lines dedicated to digital Input/Output. These lines are grouped into up to seven 8 bit I/O Ports and can be configured on a bit basis under software control to provide timing, status signals, an address/data bus for interfacing external memory, timer inputs and outputs, analog inputs, external interrupts and serial or parallel I/O with or without handshake.

Figure 3. ST90E40 Block Diagram



GENERAL DESCRIPTION (Continued)

Three basic memory spaces are available to support this wide range of configurations: Program Memory (internal and external), Data Memory (external) and the Register File, which includes the control and status registers of the on-chip peripherals.

Two 16 bit MultiFunction Timers, each with an 8 bit Prescaler and 13 operating modes allow simple use for complex waveform generation and measurement, PWM functions and many other systemmsiming functions by the usage of the two associated DMA channels for each timer.

In addition there is an 8 channel Analog to Digital Converter with integral sample and hold, fast 11µs conversion time and 8 bit resolution. An Analog Watchdog feature is included for two input channels.

Completing the device is a full duplex Serial Communications Interface with an integral 110 to 375,000 baud rate generator, asynchronous and 1.5Mbyte/s synchronous capability (fully programmable format) and associated address/wake-up option, plus two DMA channels.

1.2 PIN DESCRIPTION

$\overline{AS}$. *Address Strobe (output, active low, 3-state).* Address Strobe is pulsed low once at the beginning of each memory cycle. The rising edge of $\overline{AS}$ indicates that address, Read/Write (R/$\overline{W}$), and Data Memory signals are valid for program or data memory transfers. Under program control, $\overline{AS}$ can be placed in a high-impedance state along with Port 0 and Port 1, Data Strobe ($\overline{DS}$) and R/$\overline{W}$.

$\overline{DS}$. *Data Strobe (output, active low, 3-state).* Data Strobe provides the timing for data movement to or from Port 0 for each memory transfer. During a write cycle, data out is valid at the leading edge of $\overline{DS}$. During a read cycle, Data In must be valid prior to the trailing edge of $\overline{DS}$. When the ST9040 accesses on-chip memory, $\overline{DS}$ is held high during the whole memory cycle. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and R/$\overline{W}$.

R/$\overline{W}$. *Read/Write (output, 3-state).* Read/Write determines the direction of data transfer for external memory transactions. R/$\overline{W}$ is low when writing to external program or data memory, and high for all other transactions. It can be placed in a high impedance state along with Port 0, Port 1, $\overline{AS}$ and $\overline{DS}$.

$\overline{RESET}$/V_{PP}. *Reset (input, active low) or V_{PP} (input).* The ST9 is initialised by the Reset signal. With the deactivation of $\overline{RESET}$, program execution begins from the Program memory location pointed to by the vector contained in program memory locations 00h and 01h. In the EPROM programming Mode, this pin acts as the programming voltage input VPP.

OSCIN, OSCOUT. *Oscillator (input and output).* These pins connect a parallel-resonant crystal (24MHz maximum), or an external source to the on-chip clock oscillator and buffer. OSCIN is the input of the oscillator inverter and internal clock generator; OSCOUT is the output of the oscillator inverter.

AV_{DD}. Analog V_{DD} of the Analog to Digital Converter.

AV_{SS}. Analog V_{SS} of the Analog to Digital Converter. *Must be tied to V_{SS}.*

V_{DD}. Main Power Supply Voltage (5V ± 10%)

V_{SS}. Digital Circuit Ground.

P0.0-P0.7, P1.0-P1.7, P2.0-P2.7 P3.0-P3.7, P4.0-P4.7, P5.0-P5.7, P7.0-P7.7 *I/O Port Lines (Input/Output, TTL or CMOS compatible).* 56 lines grouped into I/O ports of 8 bits, bit programmable under program control as general purpose I/O or as alternate functions.

1.3 I/O PORT ALTERNATE FUNCTIONS

Each pin of the I/O ports of the ST90E40/T40 may assume software programmable Alternative Functions as shown in the Pin Configuration Tables. Due to Bonding options for the packages, some functions may not be present, Table 3 shows the Functions allocated to each I/O Port pin and a summary of packages for which they are available.

PIN DESCRIPTION (Continued)

Table 3. ST90E40, T40 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port. bit				PLCC	PQFP
P0.0	A0/D0	I/O	Address/Data bit 0 mux	24	39
P0.1	A1/D1	I/O	Address/Data bit 1 mux	25	40
P0.2	A2/D2	I/O	Address/Data bit 2 mux	26	41
P0.3	A3/D3	I/O	Address/Data bit 3 mux	27	42
P0.4	A4/D4	I/O	Address/Data bit 4 mux	28	43
P0.5	A5/D5	I/O	Address/Data bit 5 mux	29	44
P0.6	A6/D6	I/O	Address/Data bit 6 mux	30	45
P0.7	A7/D7	I/O	Address/Data bit 7 mux	31	46
P1.0	A8	O	Address bit 8	23	38
P1.1	A9	O	Address bit 9	22	37
P1.2	A10	O	Address bit 10	21	36
P1.3	A11	O	Address bit 11	20	35
P1.4	A12	O	Address bit 12	19	34
P1.5	A13	O	Address bit 13	18	33
P1.6	A14	O	Address bit 14	17	31
P1.7	A15	O	Address bit 15	16	30
P2.0	NMI	I	Non-Maskable Interrupt	44	64
P2.0	ROMless	I	ROMless Select (Mask option)	44	64
P2.1	P/$\overline{D}$	O	Program/Data Space Select	45	65
P2.1	SDI	I	SPI Serial Data Out	45	65
P2.2	INT2	I	External Interrupt 2	46	66
P2.2	SCK	O	SPI Serial Clock	46	66
P2.3	SDO	O	SPI Serial Data In	47	67
P2.4	INT1	I	External Interrupt 1	48	68
P2.4	$\overline{WRSTB5}$	I	Handshake Write Strobe P5	48	68
P2.5	WRRDY5	O	Handshake Write Ready P5	49	69
P2.6	INT3	I	External Interrupt 3	50	70
P2.6	$\overline{RDSTB5}$	I	Handshake Read Strobe P5	50	70
P2.6	P/$\overline{D}$	O	Program/Data Space Select	50	70
P2.7	RDRDY5	O	Handshake Read Ready P5	51	71
P3.0	T0INA	I	MF Timer 0 Input A	15	29
P3.0	P/$\overline{D}$	O	Program/Data Space Select	15	29
P3.1	T0OUTA	O	MF Timer 0 Output A	14	28
P3.2	T0INB	I	MF Timer 0 Input B	13	27
P3.3	T0OUTB	O	MF Timer 0 Output B	12	26
P3.4	T1INA	I	MF Timer 1 Input A	11	25

PIN DESCRIPTION (Continued)

Table 4. ST90E40, T40 I/O Port Alternate Function Summary

I/O PORT	Name	Function	Alternate Function	Pin Assignment	
Port. bit				PLCC	PQFP
P3.5	T1OUTA	O	MF Timer 1 Output A	10	24
P3.6	T1INB	I	MF Timer 1 Input B	9	23
P3.7	T1OUTB	O	MF Timer 1 Output B	8	22
P4.0	Ain0	I	A/D Analog Input 0	52	72
P4.1	Ain1	I	A/D Analog Input 1	53	73
P4.2	Ain2	I	A/D Analog Input 2	54	74
P4.3	Ain3	I	A/D Analog Input 3	55	75
P4.4	Ain4	I	A/D Analog Input 4	61	4
P4.5	Ain5	I	A/D Analog Input 5	56	76
P4.6	Ain6	I	A/D Analog Input 6	57	77
P4.7	Ain7	I	A/D Analog Input 7	58	78
P5.0		I/O	I/O Handshake Port 5	3	15
P5.1		I/O	I/O Handshake Port 5	2	14
P5.2		I/O	I/O Handshake Port 5	1	13
P5.3		I/O	I/O Handshake Port 5	68	11
P5.4		I/O	I/O Handshake Port 5	65	8
P5.5		I/O	I/O Handshake Port 5	64	7
P5.6		I/O	I/O Handshake Port 5	63	6
P5.7		I/O	I/O Handshake Port 5	62	5
P7.0	SIN	I	SCI Serial Input	43	61
P7.1	SOUT	O	SCI Serial Output	42	60
P7.1	ROMless	I	ROMless Select (Mask option)	42	60
P7.2	INT4	I	External Interrupt 4	41	59
P7.2	TXCLK	I	SCI Transmit Clock Input	41	59
P7.2	CLKOUT	O	SCI Byte Sync Clock Output	41	59
P7.3	INT5	I	External Interrupt 5	40	58
P7.3	RXCLK	I	SCI Receive Clock Input	40	58
P7.3	ADTRG	I	A/D Conversion Trigger	40	58
P7.4	INT6	I	External Interrupt 6	39	57
P7.4	P/$\overline{D}$	O	Program/Data Space Select	39	57
P7.5	$\overline{WAIT}$	I	External Wait Input	38	56
P7.6	WDOUT	O	T/WD Output	37	55
P7.6	$\overline{BUSREQ}$	I	External Bus Request	37	55
P7.7	WDIN	I	T/WD Input	36	54
P7.7	$\overline{BUSACK}$	O	External Bus Acknowledge	36	54

1.4 MEMORY

The memory of the ST90E40 is functionally divided into two areas, the Register File and Memory. The Memory is divided into two spaces, each having a maximum of 65,536 bytes. The two memory spaces are separated by function, one space for Program code, the other for Data. The ST90E40 16K bytes of on-chip EPROM memory are selected at memory addresses 0 through 3FFFh (hexadecimal) in the PROGRAM space, while the ST90T40 OTP version has the top 64 bytes of the EPROM reserved by SGS-THOMSON for testing purposes. The DATA space includes the 512 bytes of on-chip EEPROM at addresses 0 through 1FFh and the 256 bytes of on-chip RAM memory at memory addresses 200h through 2FFh.

WARNING. *The ST90T40 has its 64 upper bytes in the internal EPROM reserved for testing purpose.*

External memory may be addressed using the multiplexed address and data buses (Alternate Functions of Ports 0 and 1). At addresses greater than the first 16K of program space, the ST90E40 executes external memory cycles for instruction fetches. Additional Data Memory may be decoded externally by using the P/$\overline{D}$ Alternate Function output. The on-chip general purpose (GP) Registers may also be used as RAM memory for minimum chip count systems.

1.5 EPROM PROGRAMMING

The 16384 bytes of EPROM memory of the ST90E40 (16320 for the ST90T40) may be programmed by using the EPROM Programming Boards (EPB) available from SGS-THOMSON.

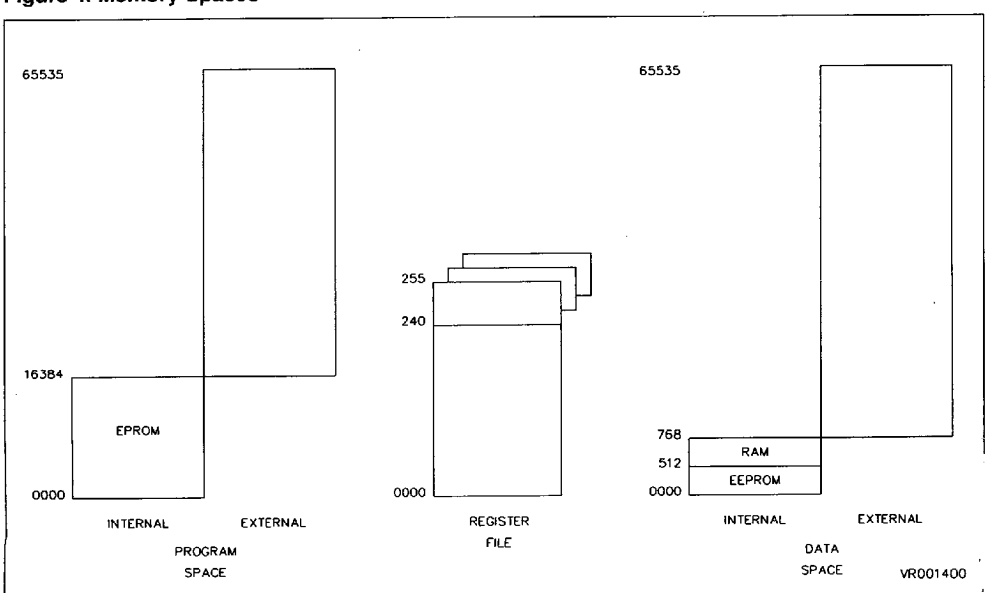
1.5.1 Eprom Erasing

The EPROM of the windowed package of the ST90E40 may be erased by exposure to Ultra-Violet light.

The erasure characteristic of the ST90E40 is such that erasure begins when the memory is exposed to light with a wave lengths shorter than approximately 4000Å. It should be noted that sunlight and some types of fluorescent lamps have wavelengths in the range 3000-4000Å. It is thus recommended that the window of the ST90E40 packages be covered by an opaque label to prevent unintentional erasure problems when testing the application in such an environment.

The recommended erasure procedure of the EPROM is the exposure to short wave ultraviolet light which have a wave-length 2537Å. The integrated dose (i.e. U.V. intensity x exposure time) for erasure should be a minimum of 15W-sec/cm2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000µW/cm^2 power rating. The ST90E40 should be placed within 2.5cm (1Inch) of the lamp tubes during erasure.

Figure 4. Memory Spaces



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{DD}	Supply Voltage	– 0.3 to 7.0	V
AV_{DD}, AV_{SS}	Analog Supply Voltage	$V_{SS} = AV_{SS} < AV_{DD} \leq V_{DD}$	V
V_I	Input Voltage	– 0.3 to V_{DD} +0.3	V
V_O	Output Voltage	– 0.3 to V_{DD} +0.3	V
V_{PP}	Input Voltage on V_{PP} Pin	-0.3 to 13.5	V
T_{STG}	Storage Temperature	– 55 to + 150	°C
I_{INJ}	Pin Injection Current Digital	-5 to 5	mA
I_{INJ}	Pin Injection Current Analog	-5 to 5	mA
	Maximum accumulated pin injection Current in the device	-50 to 50	mA

Note: Stresses above those listed as "absolute maximum ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability. All voltages are referenced to VSS

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value		Unit
		Min.	Max.	
T_A	Operating Temperature	– 40	85	°C
V_{DD}	Operating Supply Voltage	4.5	5.5	V
f_{OSCE}	External Oscillator Frequency		24	MHz
f_{OSCI}	Internal Clock Frequency (INTCLK)		12	MHz

DC ELECTRICAL CHARACTERISTICS

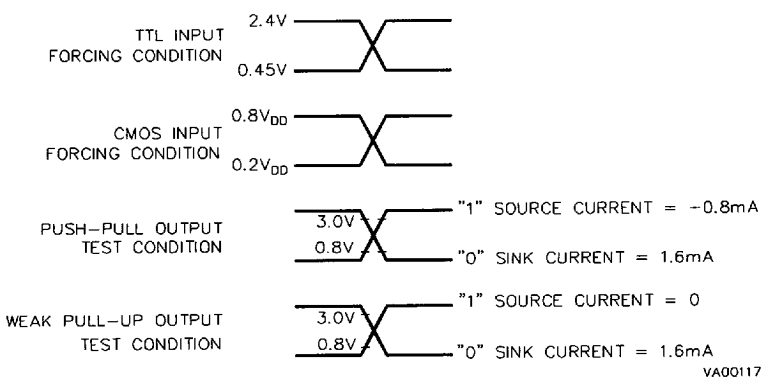
(V_{DD} = 5V ± 10% T_A = – 40°C to + 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
V_{IHCK}	Clock Input High Level	External Clock	0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILCK}	Clock Input Low Level	External Clock	– 0.3		0.3 V_{DD}	V
V_{IH}	Input High Level	TTL	2.0		V_{DD} + 0.3	V
		CMOS	0.7 V_{DD}		VDD + 0.3	V
V_{IL}	Input Low Level	TTL	– 0.3		0.8	V
		CMOS	– 0.3		0.3 V_{DD}	V
V_{IHRS}	$\overline{\text{RESET}}$ Input High Level		0.7 V_{DD}		V_{DD} + 0.3	V
V_{ILRS}	$\overline{\text{RESET}}$ Input Low Level		–0.3		0.3 V_{DD}	V
V_{HYRS}	$\overline{\text{RESET}}$ Input Hysteresis		0.3		1.5	V
V_{OH}	Output High Level	Push Pull, Iload = – 0.8mA	V_{DD} – 0.8			V
V_{OL}	Output Low Level	Push Pull or Open Drain, Iload = 1.6mA			0.4	V

DC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{WPU}	Weak Pull-up Current	Bidirectional Weak Pull-up, V_{OL} = 0V	– 50	– 200	– 420	µA
I_{APU}	Active Pull-up Current, for INT0 and INT7 only	V_{IN} < 0.8V, under Reset	– 80	– 200	– 420	µA
I_{LKIO}	I/O Pin Input Leakage	Input/Tri-State, 0V < V_{IN} < V_{DD}	– 10		+ 10	µA
I_{LKRS}	$\overline{\text{Reset}}$ Pin Input Leakage	0V < V_{IN} < V_{DD}	– 30		+ 30	µA
I_{LKAD}	A/D Pin Input Leakage	Alternate Function, Open Drain, 0V < V_{IN} < V_{DD}	– 13		+13	µA
I_{LKAP}	Active Pull-up Input Leakage	0V < V_{IN} < 0.8V	– 10		+ 10	µA
I_{LKOS}	OSCIN Pin Input Leakage	0V < V_{IN} < V_{DD}	– 10		+ 10	µA
V_{PP}	EPROM Programming Voltage		12.2	12.5	12.8	V
I_{PP}	EPROM Programming Current				30	mA

DC TEST CONDITIONS

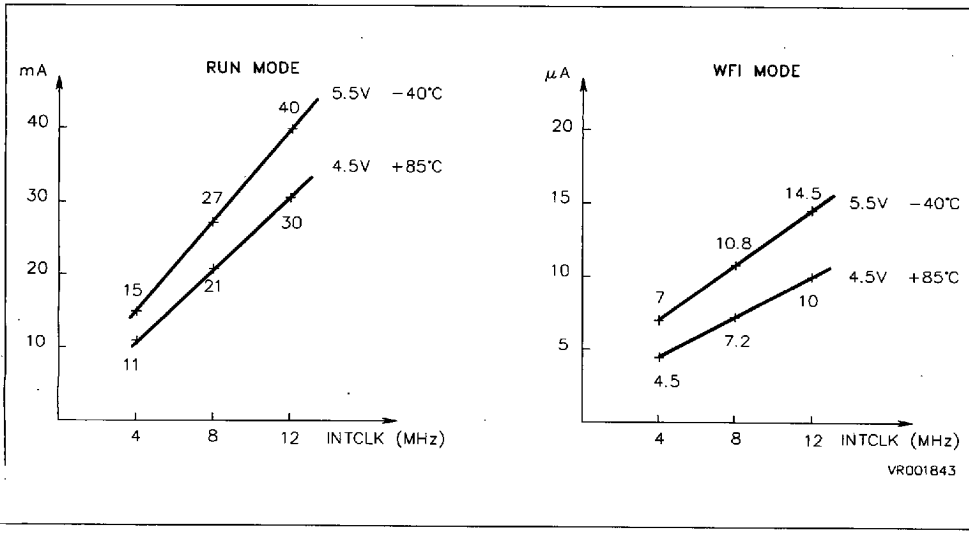


AC ELECTRICAL CHARACTERISTICS

(V_{DD} = 5V ± 10% T_A = – 40°C to + 85°C, unless otherwise specified)

Symbol	Parameter	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
I_{DD}	Run Mode Current no CPUCLK prescale, Clock divide by 2	24MHz		40	70	mA
I_{DP2}	Run Mode Current Prescale by 2 Clock divide by 2	24MHz		19	40	mA
I_{WFI}	WFI Mode Current no CPUCLK prescale, Clock divide by 2	24MHz		15	20	mA
I_{HALT}	HALT Mode Current	24MHz		50	100	µA

Typical Current Versus Frequency of Operation (fosc)



CLOCK TIMING TABLE

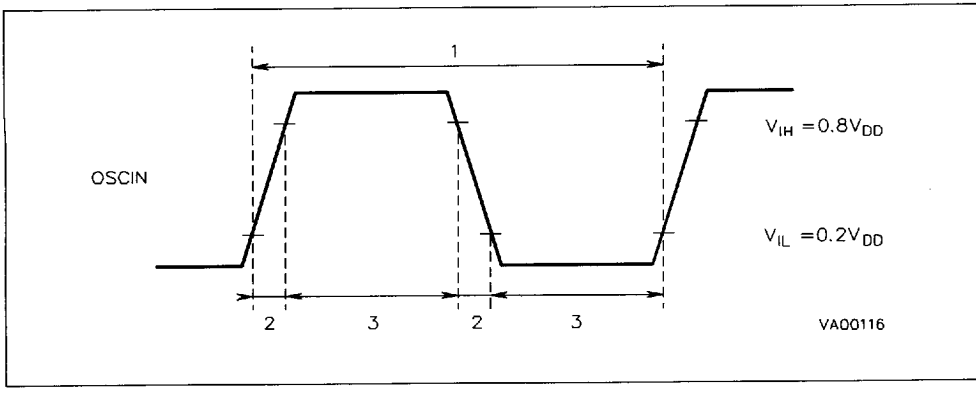
(V_{DD} = 5V ± 10%, T_A = − 40°C to + 85°C, INTCLK = 12MHz, unless otherwise specified

N°	Symbol	Parameter	Value		Unit	Note
			Min.	Max.		
1	TpC	OSCIN Clock Period	41.5		ns	1
			83		ns	2
2	TrC, TfC	OSCIN Rise and Fall Time		12	ns	
3	TwCL, TwCH	OSCIN Low and High Width	17	25	ns	1
			38		ns	2

Notes:

1. Clock divided by 2 internally (MODER.DIV2=1)
2. Clock not divided by 2 internally (MODER.DIV2=0)

CLOCK TIMING



EXTERNAL BUS TIMING TABLE (V_{DD} = 5V ± 10%, T_A = – 40°C to + 85°C, Cload = 50pF, CPUCLK = 12MHz, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TsA (AS)	Address Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TWCH+PTpC –18	20		ns
2	ThAS (A)	Address Hold Time after $\overline{AS}$ ↑	TpC –17	TwCL –13	25		ns
3	TdAS (DR)	$\overline{AS}$ ↑ to Data Available (read)	TpC (4P+2W+4) –52	TpC (2P+W+2) –51		115	ns
4	TwAS	$\overline{AS}$ Low Pulse Width	TpC (2P+1) –7	TwCH+PTpC –3	35		ns
5	TdAz (DS)	$\overline{DS}$ ↓ to Address Float			12		ns
6	TwDSR	$\overline{DS}$ Low Pulse Width (read)	TpC (4P+2W+3) –20	TwCH+TpC (2P+W+1) –16	105		ns
7	TwDSW	$\overline{DS}$ Low Pulse Width (write)	TpC (2P+2W+2) –13	TpC (P+W+1) –13	70		ns
8	TdDSR (DR)	$\overline{DS}$ ↓ to Data Valid Delay (read)	TpC (4P+2W-3) –50	TwCH+TpC(2P+W+1) –46		75	ns
9	ThDR (DS)	Data to $\overline{DS}$ ↑ Hold Time (read)	0	0	0		ns
10	TdDS (A)	$\overline{DS}$ ↑ to Address Active Delay	TpC –7	TwCL –3	35		ns
11	TdDS (AS)	$\overline{DS}$ ↑ to $\overline{AS}$ ↓ Delay	TpC –18	TwCL –14	24		ns
12	TsR/W (AS)	R/$\overline{W}$ Set-up Time before $\overline{AS}$ ↑	TpC (2P+1) –22	TwCH+PTpC –18	20		ns
13	TdDSR (R/W)	$\overline{DS}$ ↑ to R/$\overline{W}$ and Address Not Valid Delay	TpC –9	TwCL –5	33		ns
14	TdDW (DSW)	Write Data Valid to $\overline{DS}$ ↓ Delay (write)	TpC (2P+1) –32	TwCH+PTpC –28	10		ns
15	ThDS (DW)	Data Hold Time after $\overline{DS}$ ↑ (write)	TpC –9	TwCL –5	33		ns
16	TdA (DR)	Address Valid to Data Valid Delay (read)	TpC (6P+2W+5) –68	TwCH+TpC (3P+W+2) –64		140	ns
17	TdAs (DS)	$\overline{AS}$ ↑ to $\overline{DS}$ ↓ Delay	TpC –18	TwCL –14	24		ns

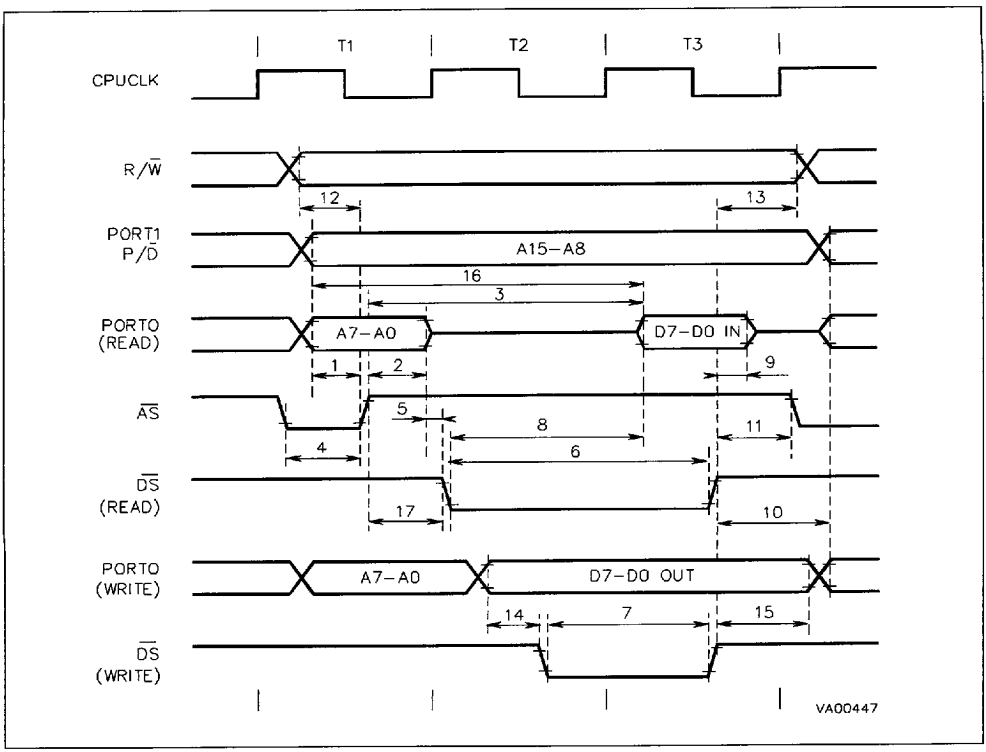
EXTERNAL WAIT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdAs (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Delay	2(P+1)TpC –29	2(P+1)TpC –29		40	ns
2	TdAs (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Min. Delay	2(P+W+1)TpC –4	2(P+W+1)TpC –4	80		ns
3	TdAs (WAIT)	$\overline{AS}$ ↑ to $\overline{WAIT}$ ↓ Max. Delay	2(P+W+1)TpC –29	2(P+W+1)TpC –29		83W+40	ns

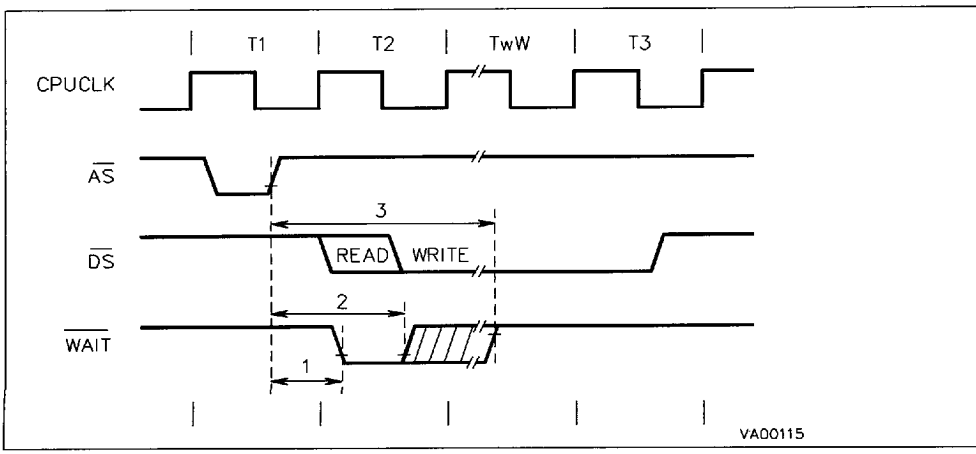
Note: (for both table) The value in the left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value in the right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

Legend:
P = Clock Prescaling Value
W = Wait Cycles
TpC =OSCIN Period
TwCH =High Level OSCIN half period
TwCL =Low Level OSCIN half period

EXTERNAL BUS TIMING



EXTERNAL WAIT TIMING



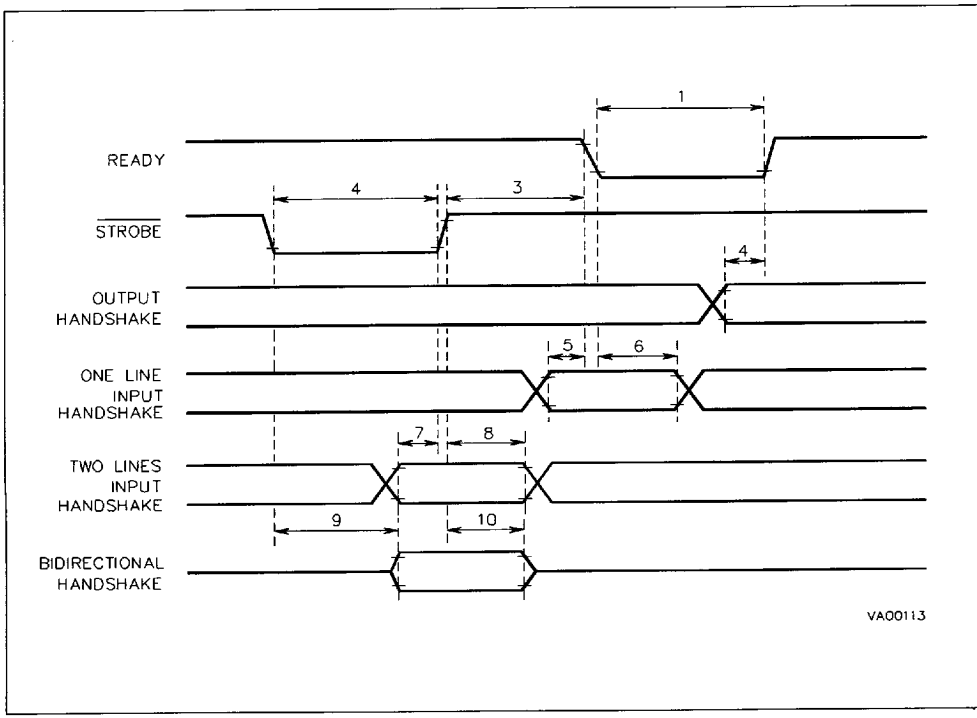
HANDSHAKE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Min.	Max.	Unit
			OSCIN Divided By 2		OSCIN Not Divided By 2				
			Min.	Max.	Min.	Max.			
1	TwRDY	RDRDY, WRRDY Pulse Width in One Line Handshake	2TpC (P+W+1) –18		TpC (P+W+1) – 18		65		ns
2	TwSTB	$\overline{RDSTB}$, $\overline{WRSTB}$ Pulse Width	2TpC+12		TpC+12		95		ns
3	TdST (RDY)	$\overline{RDSTB}$, or $\overline{WRSTB}$ ↑ to RDRDY or WRRDY ↓		TpC+45		(TpC-TwCL) +45		87	ns
4	TsPD (RDY)	Port Data to RDRDY ↑ Set-up Time	(2P+2W+1) TpC –25		TwCH+ (W+P) TpC –25		16		ns
5	TsPD (RDY)	Port Data to WRRDY ↓ Set-up Time in One Line Handshake	43		43		43		ns
6	ThPD (RDY)	Port Data to WRRDY ↓ Hold Time in One Line Handshake	0		0		0		ns
7	TsPD (STB)	Port Data to $\overline{WRSTB}$ ↑ Set-up Time	10		10		10		ns
8	ThPD (STB)	Port Data to WRSTB ↑ Hold Time	25		25		25		ns
9	TdSTB (PD)	$\overline{RDSTBD}$ ↑ to Port Data Delay Time in Bidirectional Handshake		35		35		35	ns
10	TdSTB (PHZ)	$\overline{RDSTB}$ ↑ to Port High-Z Delay Time in Bidirectional Handshake		25		25		25	ns

Note: The value in the left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value in the right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescaler value of zero and zero wait status.

legend:
F = Clock Prescaling Value (R235.4,3,2)
= Programmable Wait Cycles (R252.2.1.0/5,4,3) + External Wait Cycles

HANDSHAKE TIMING

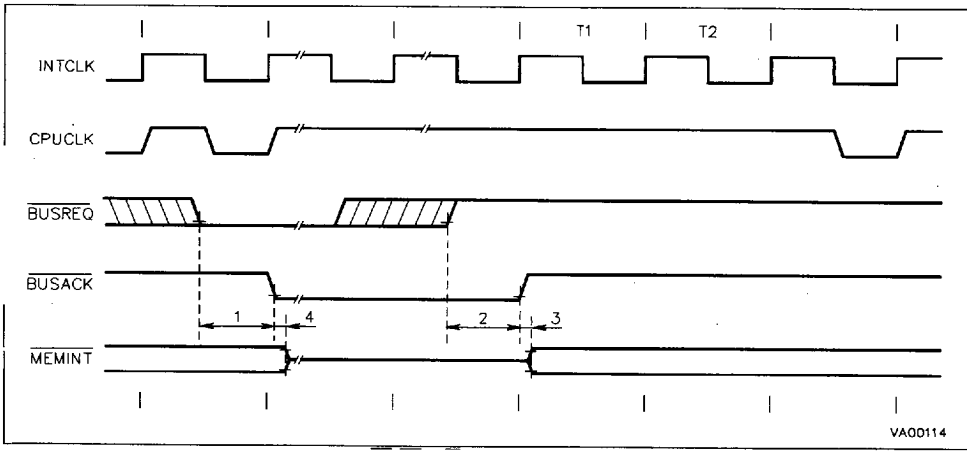


BUS REQUEST/ACKNOWLEDGE TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2	OSCIN Not Divided By 2	Min.	Max.	
1	TdBR (BACK)	$\overline{BREQ}$ ↓ to $\overline{BUSACK}$ ↓	TpC+8	TwCL+12	50		ns
			TpC(6P+2W+7)+65	TpC(3P+W+3)+TwCL+65		360	ns
2	TdBR (BACK)	$\overline{BREQ}$ ↑ to $\overline{BUSACK}$ ↑	3TpC+60	TpC+TwCL+60		185	ns
3	TdBACK (BREL)	$\overline{BUSACK}$ ↓ to Bus Release	20	20		20	ns
4	TdBACK (BACT)	$\overline{BUSACK}$ ↑ to Bus Active	20	20		20	ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24MHz divided by 2, prescale value of zero and zero wait status.

BUS REQUEST/ACKNOWLEDGE TIMING



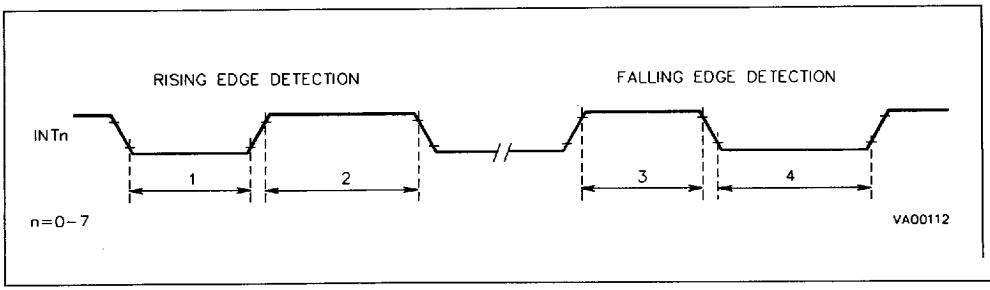
Note : MEMINT = Group of memory interface signals: $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$, P00-P07, P10-P17

EXTERNAL INTERRUPT TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Value (Note)				Unit
			OSCIN Divided By 2 Min.	OSCIN Not Divided By 2 Min.	Min.	Max.	
1	TwLR	Low Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
2	TwHR	High Level Minimum Pulse Width in Rising Edge Mode	2TpC+12	TpC+12	95		ns
3	TwHF	High Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns
4	TwLF	Low Level Minimum Pulse Width in Falling Edge Mode	2TpC+12	TpC+12	95		ns

Note: The value left hand two columns show the formula used to calculate the timing minimum or maximum from the oscillator clock period, prescale value and number of wait cycles inserted.
The value right hand two columns show the timing minimum and maximum for an external clock at 24 MHz divided by 2, prescale value of zero and zero wait status.

EXTERNAL INTERRUPT TIMING

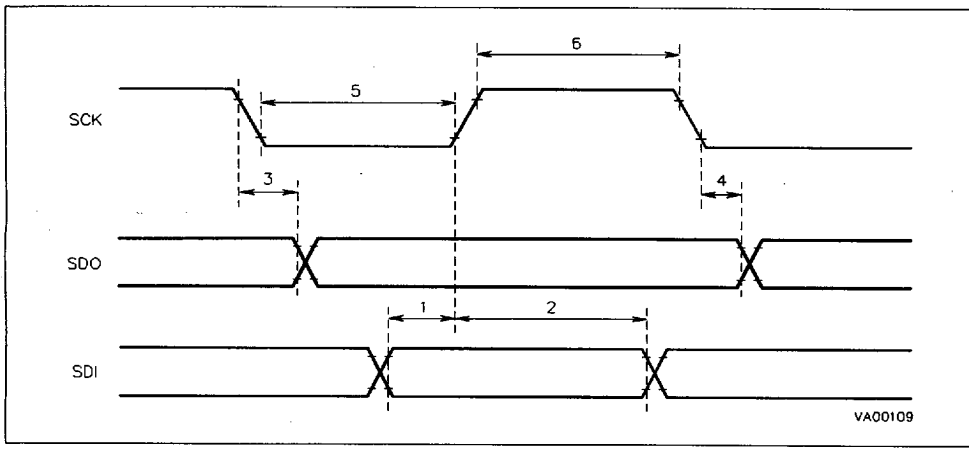


SPI TIMING TABLE (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF, INTCLK = 12MHz, Output Alternate Function set as Push-pull)

N°	Symbol	Parameter	Value		Unit
			Min.	Max.	
1	TsDI	Input Data Set-up Time	100		ns
2	ThDI (1)	Input Data Hold Time	1/2 TpC+100		ns
3	TdOV	SCK to Output Data Valid		100	ns
4	ThDO	Output Data Hold Time	-20		ns
5	TwSKL	SCK Low Pulse Width	300		ns
6	TwSKH	SCK High Pulse Width	300		ns

Note: 1. TpC is the OSCIN Clock period.

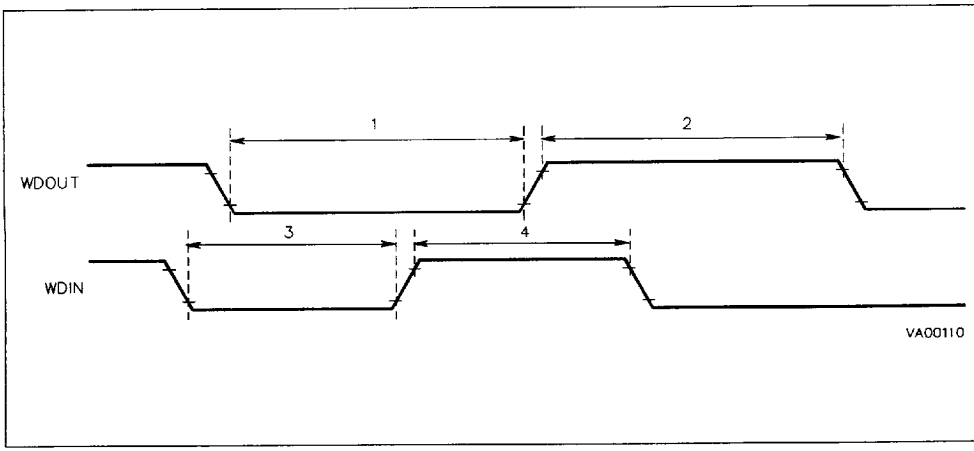
SPI TIMING



WATCHDOG TIMING TABLE(V_{DD} = 5V ± 10%, T_A = – 40°C to +85°C, Cload = 50pF, CPUCLK = 12MHz, Push-pull output configuration, unless otherwise specified)

N°	Symbol	Parameter	Values		Unit
			Min.	Max.	
1	TwWDOL	WDOUT Low Pulse Width	620		ns
2	TwWDOH	WDOUT High Pulse Width	620		ns
3	TwWDIL	WDIN High Pulse Width	350		ns
4	TwWDIH	WDIN Low Pulse Width	350		ns

WATCHDOG TIMING



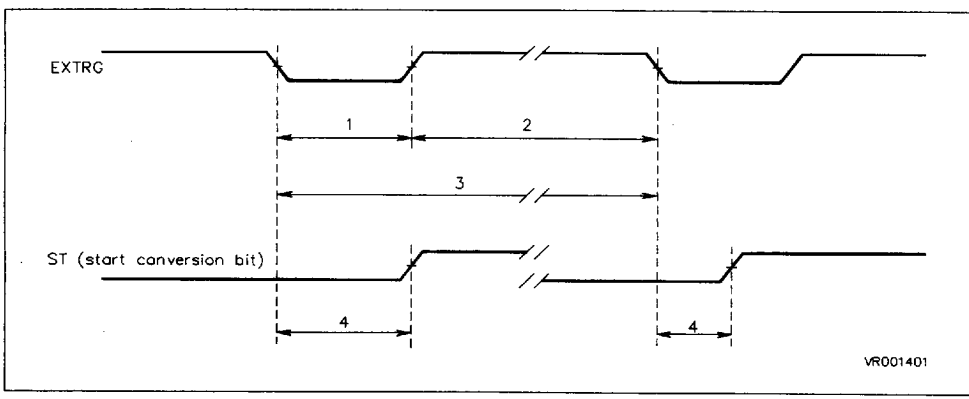
A/D CONVERTER

EXTERNAL TRIGGER TIMING (V_{DD} = 5V ± 10%, T_A = –40°C to +85°C, Cload = 50pF)

N°	Symbol	Parameter	Oscin divided by 2 (1)		Oscin not divided (1)		Value(2)		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
1	T_{LOW}	External Trigger pulse width	$2xT_{PC}$		T_{PC}		83		ns
2	T_{HIGH}	External Trigger pulse	$2xT_{PC}$		T_{PC}		83		ns
3	T_{EXT}	External trigger active edges distance	$138xT_{PC}$		$69xT_{PC}$		5.75		µs
4	T_{STR}	Internal delay between EXTRG falling edge and first conversion start	T_{PC}	$3xT_{PC}$	0.5xTPC	$1.5xT_{PC}$	41.5	125	ns

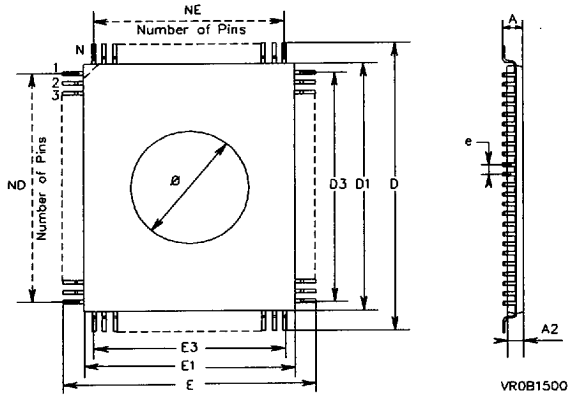
Notes:
1. Variable clock (TPC=OSCIN clock period)
2. INTCLK=12MHz

A/D External Trigger Timing



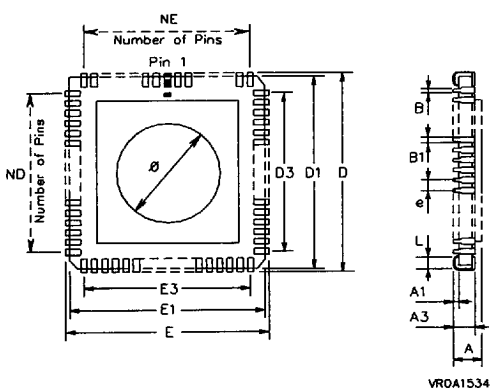
PACKAGE MECHANICAL DATA

80-Pin Ceramic Quad Flat Package with Window



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		3.55			0.14	
A2		3.40			0.133	
D		23.90			0.941	
D1		20.00			0.787	
D3		18.40			0.724	
E		17.90			0.705	
E1		14.00			0.551	
E3		12.00			0.472	
Ø		7.62			0.3	
e		0.80			0.032	
Number of Pins						
N	80					
ND	24					
NE	16					

68-Pin Ceramic Leadless Chip Carrier with Window



Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A		4.47			0.176	
A1		0.89			0.035	
A3		-			-	
B		0.48			0.019	
B1		-			-	
D		25.1			0.990	
D1		23.6			0.930	
D3		20.3			0.800	
E		25.1			0.990	
E1		23.6			0.930	
E3		20.3			0.800	
Ø		8			0.32	
e		1.27			0.050	
Number of Pins						
N	64					
ND	16					
NE	16					

ORDERING INFORMATION

Sales Type	Frequency	Temperature Range	Package
ST90E40L1/ES[1]	24MHz	0°C to + 70°C	CLCC68W
ST90E40G1/ES[1]		0°C to + 70°C	CQFP80W
ST90T40C6	24MHz	-40°C to + 85°C	PLCC68
ST90T40Q1		0°C to + 70°C	PQFP80

Note . EPROM parts are tested at 25°C only